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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,305	02/28/2002	Stephen M. Trimberger	X-874 US	7532

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,305	TRIMBERGER, STEPHEN M.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-26 and 28-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-24* is/are allowed.

6)☒ Claim(s) *1-4,6-19,25,26 and 28-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to Amendment filed 6/16/2005. Claims 20-24 are allowed. Claims 1-4, 6-19, 25, 26 and 28-39 are rejected. Claims 5 and 27 have been cancelled. Claims 1-4, 6-26 and 28-39 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-19, 25, 26 and 28-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Charlton et al. (US Patent No. 6,289,292) in view of MacArthur (U.S. Patent No. 5,925,920).

Regarding independent Claims 1, 25, Charlton substantially discloses a system and a method for identification of electronic components based on their physical characteristics, including a characterization value test station for determining the characterization values of the components pursuant to the characterization function, and a data base which stores information that pertains to each component with the component's characterization value linked as an identifier to the information, wherein information pertaining to a component may be retrieved from the database based on the

component's characterization value, see Abstract and Summary of the Invention, comprising:

Testing a plurality of memory devices (16a-d) of memory 15 in a memory module, Figures 2 and 5, and for each memory device 16 from a set of memory devices (16a-d), using the memory tester to determine a device's characterization value and tests the device for bit defects.

Recording defect data for each defective memory device (16a-d), wherein as disclosed, "the bit defect information and characterization value are stored together in a database record to link the characterization value as an identifier to the bit defect information. After all of the devices have been tested and linked to their characterization value, they can then be combined and distributed for manufacturing or other processes without requiring any added marks or identification materials".

Receiving and providing from and to a user, respectively, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

With respect to programmable logic devices (PLD) being under test, according to Charlton, Memory devices under test may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

With respect to new claimed limitation of "defective PLD having the first identifier", Charlton discloses bit defect information of an electronic component with an associated identifier stored together in a database record, which links the identifier to the bit defect information of the electronic component.

However, Charlton does not explicitly disclose, "implementing a user design in a first defective PLD having the first identifier", as amended.

In an analogous art, MacArthur discloses implementing a user design in a Programmable Logic Device (PLD), by having the user input a logic circuit design into a computer using one of a variety of design entry options. After the logic circuit design is entered into the computer, the computer maps the logic circuit design into the programmable logic device in order to implement the logic circuit design when programmed. Furthermore, MacArthur recognizes during the manufacturing and testing of a programmable logic device, the device may be found to have a defective programmable element. Therefore, MacArthur provides redundant routing resources in the (PLD) to reduce the probability of producing defective programmable logic devices (see, Col. 2, lines 3-35).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement a user design in a defective electronic component, such as a defective PROM (programmable read only memory) of Charlton by mapping the logic circuit design into the PROM using redundant routing resources, as taught by MacArthur, for the purpose of correcting such a defect, since it reduces the probability of producing defective programmable logic devices.

Regarding Claims 2, 26, Charlton discloses receiving an identifier (component's characterization value) from a user (manufacturer), and providing to the manufacturer the component's bit defect information from the database via the data communications link, which is the link between the characterization value test station 50 and a personal computer 35 for monitoring and controlling test station 50.

Regarding Claims 3, 4, Charlton discloses wherein the location information, such as the bit error information (i.e., defect locations) of memory 15 is available to memory recovery interface 12, which provides to host processor 14 access to memory 15 without alteration of the processor's addressing scheme, while preventing any defective memory cells/bytes of memory 15 from being used. The bit error information is provided to memory recovery interface 12 through EPROM 13 (e.g., the information could be downloaded into internal memory of memory recovery interface 12 during start-up).

Regarding Claims 6, 28, Charlton discloses receiving and providing from and to a user, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

Regarding Claims 7, 29, Charlton discloses with respect to a PLD being field programmable gate array (FPGA), according to Charlton Memory devices under test

may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

Regarding Claims 8, Charlton discloses maintaining the database for storing the bit defect information and the characterization value which links the characterization value as an identifier to the bit defect information, including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Regarding Claims 30-32, Charlton discloses device specific information comprising a database for storing the bit defect information and the characterization value which links the characterization value as an identifier to the bit defect information, including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Regarding independent Claims 9, 33, Charlton discloses the common limitations as described in the independent claim 1, above, comprising:

Receiving and providing from and to a user, respectively, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

With respect to programmable logic devices (PLD) being under test, according to Charlton Memory devices under test may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

Charlton does not explicitly disclose, "implementing the user design in the first PLD using the device specific information for the first PLD".

In an analogous art, MacArthur discloses implementing a user design in a Programmable Logic Device (PLD), by having the user input a logic circuit design into a computer using one of a variety of design entry options. After the logic circuit design is entered into the computer, the computer maps the logic circuit design into the programmable logic device in order to implement the logic circuit design when programmed. Furthermore, MacArthur recognizes during the manufacturing and testing of a programmable logic device, the device may be found to have a defective programmable element. Therefore, MacArthur provides redundant routing resources in the (PLD) to reduce the probability of producing defective programmable logic devices (see, Col. 2, lines 3-35).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement a user design in a defective electronic component, such as a defective PROM (programmable read only memory) of Charlton by mapping the logic circuit design into the PROM using redundant routing resources, as taught by MacArthur, for the purpose of correcting such a defect, since it reduces the probability of producing defective programmable logic devices.

Regarding Claims 10, 34, Charlton discloses receiving an identifier (component's characterization value) from a user (manufacturer), and providing to the manufacturer the component's bit defect information from the database via the data communications link, which is the link between the characterization value test station 50 and a personal computer 35 for monitoring and controlling test station 50.

Regarding Claims 11, 12, Charlton discloses wherein the location information, such as the bit error information (i.e., defect locations) of memory 15 is available to memory recovery interface 12, which provides to host processor 14 access to memory 15 without alteration of the processor's addressing scheme, while preventing any defective memory cells/bytes of memory 15 from being used. The bit error information is provided to memory recovery interface 12 through EPROM 13 (e.g., the information could be downloaded into internal memory of memory recovery interface 12 during start-up).

Regarding Claims 16, 36, Charlton discloses with respect to a PLD being field programmable gate array (FPGA), according to Charlton Memory devices under test

may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

Regarding Claims 17, Charlton discloses maintaining the database for storing the bit defect information and the characterization value which links the characterization value as an identifier to the bit defect information, including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Implementing a user design in a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored, then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding Claim 19, Charlton discloses implementing the user design in a defective memory device (16a-d), including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Regarding Claims 37-39, Charlton discloses device specific information comprising a database for storing the bit defect information and the characterization

value which links the characterization value as an identifier to the bit defect information, including generating a bit error map which can then be utilized as an identifier to store and retrieve the entire test information file for the component from a database. Generating a constraints file for memory devices using memory test station 20, which tests and maps memory devices for bit errors, as well as determines characterization values for each device, Figures 4A and 4B.

Regarding Claims 13-15, 18 and 35 Charlton substantially discloses the claimed invention as applied to independent claims 9 and 33 above.

Regarding Claims 13, Charlton discloses a defective memory device (16a-d), in manufacturing a module with reference to the example of the memory device 16 for which bit defect information has been stored, then the defect information can be used to manufacture a module in which the component-specific defects are circumvented.

Regarding Claims 14, 15, Charlton discloses receiving and providing from and to a user, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

Regarding Claim 18, Charlton discloses with respect to a PLD being field programmable gate array (FPGA), according to Charlton Memory devices under test

may be, but are not limited to, PROM (programmable read only memory), or EPROM (erasable PROM).

Regarding Claims 35, Charlton discloses receiving and providing from and to a user, such as a manufacturer, an identifier corresponding to the component's characterization value to retrieve the component's bit defect information from the database, wherein as disclosed "wherever the bit defect information is required for a given component, the component's characterization value is determined and used to retrieve the component's bit defect information from the database".

Regarding Claims 13-15, 18 and 35, Charlton does not explicitly disclose, "implementing the user design in a PLD". However, in an analogous art, MacArthur discloses implementing a user design in a Programmable Logic Device (PLD), for the same obvious and motivational reasons, as described relative to the independent Claims 9 and 33, above.

Allowable Subject Matter

Claims 20-24 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention, as recited in the independent Claim 20, which includes, inter alia, the limitations of performing an incremental compilation with respect to the first design file while using the first location information to avoid the localized defects of the first defective PLD, the incremental compilation generating a second design file, and providing the second design file to the user.

Claims 21-24 are directly or indirectly depended upon claim 20 and therefore are also allowable. Therefore, claims 20-24 are allowed over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments, see Amendment, filed 6/16/2005, with respect to the rejection of claims 1-39 under 35 U.S.C. 102(e) as being anticipated by Charlton et al. (US Patent N0. 6,289,292) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground of rejection is made in view of Claims 1-4, 6-19, 25, 26 and 28-39 under 35 U.S.C. 103(a) as being unpatentable over Charlton et al. (US Patent No. 6,289,292) in view of MacArthur (U.S. Patent No. 5,925,920).

In response to Applicant's argument, regarding Claims 1 and 25, the Examiner agrees that Charlton does not explicitly disclose, "implementing a user design in a first defective PLD having the first identifier", as amended. Similarly, regarding Claims 9 and 33, Charlton fail to disclose, "implementing a user design in a first defective PLD".

However, under a new ground of rejection, MacArthur discloses implementing a user design in a Programmable Logic Device (PLD), by having the user input a logic

circuit design into a computer using one of a variety of design entry options. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of MacArthur with the Charlton reference for the obvious and motivational reasons as described in the Office Action above, with respect to independent claims 1, 9, 25 and 33.

In response to Applicant's argument, regarding Claim 20, the Examiner agrees with the Applicant that the prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention, as recited in the independent Claim 20, which includes, inter alia, the limitations of performing an incremental compilation with respect to the first design file while using the first location information to avoid the localized defects of the first defective PLD, the incremental compilation generating a second design file, and providing the second design file to the user. Therefore, independent claim 20 is allowed along with its dependent claims 21-24, for the reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: _____

Randolph Building, 401 Dulany Street,
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

Date: 27 July 2005
Office Action: Final Rejection